A 94 GHZ MONOLITHIC HIGH OUTPUT POWER AMPLIFIER*

P. Huang, E. Lin**, R. Lai, M. Biedenbender, T. W. Huang, H. Wang, C. Geiger, T. Block, and P. H. Liu

TRW Electronic Systems and Technology Division

One Space Park, Redondo Beach, CA 90278

ABSTRACT

A two-stage monolithic W-band power amplifier using 0.1-μm pseudomorphic AlGaAs/InGaAs/GaAs T-gate power HEMT process has been designed, fabricated, and tested. This MMIC PA exhibits 8 dB linear gain and a maximum output power of 300mW with 10.5% peak power-added efficiency at 94GHz. The substrate thickness is 2 mil to take advantage of lower thermal resistance as well as smaller via holes and a more compact chip layout. To our knowledge, the 300-mW output power represents the highest output power for a single W-band power amplifier chip at this frequency.

INTRODUCTION

Great effort has been spent on developing monolithic integrated circuits for millimeter wave application. Various W-band MMIC low noise amplifiers [1]-[2] and power amplifiers [3]-[6] have been successfully demonstrated using AlGaAs/InGaAs/GaAs pseudomorphic T-gate power HEMT with 0.1-μm gate length. Output power capability for W-band amplifiers has been demonstrated and enhanced in the past few years [3]-[6]. Presented in this paper is a two-stage monolithic power amplifier using the 0.1-μm power HEMT process but on a thinned 2-mil GaAs substrate. The main advantages of a thinner substrate are lower thermal resistance and the use of smaller via holes. At 94 GHz, the MMIC PA has 8 dB linear gain and 300 mW maximum output power with 10.5% peak efficiency as illustrated by the on-wafer test data and in-fixture measurements. This performance demonstrates the latest breakthrough of the output power capability for W-band MMIC amplifier.

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** E. Lin was with Electronic Systems and Technology Division, TRW. He is now with RF Wave, Inc., Torrance, CA.

DEVICE CHARACTERIZATION AND MODELING

The 0.1-μm power HEMT device development has been reported in the previous publication [7]. The key difference for the amplifier presented here is that it is processed on a 2-mil substrate. MMIC power amplifiers using 2-mil substrate have been successfully demonstrated at lower frequencies [8]. Having a thinner substrate allows for smaller via holes and lower thermal resistance. With smaller via holes, device sources can be grounded with separate vias and thus lowering the source inductance which in turns can improve the gain and power density.

Device linear model is developed by carefully fitting the FET equivalent circuit to measured small signal S-parameters to 50 GHz. In addition, simple pre-matched structures centered at 94 GHz for a single device and two devices in parallel are also designed as shown in Fig. 1. These test structures are used to verify the validity of the device model at W-band. Figure 2 shows the measured and simulated performance of the pre-matched structures. DC I-V data are used together with linear model elements to complete the Curtice-Ettenberg FET asymmetric model for predicting output power performance.

Amplifier Design

The power amplifier is a single-ended two-stage

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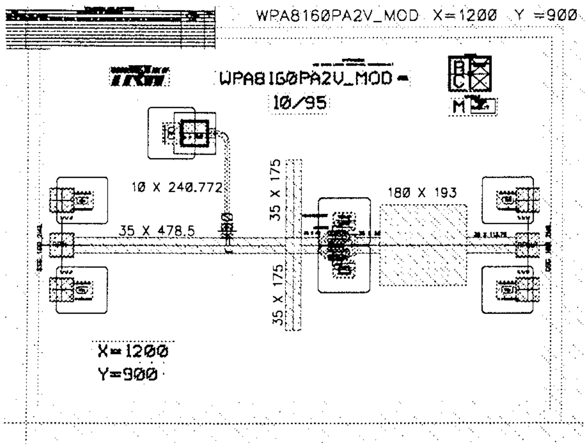

Fig. 1a Layout of the single device pre-matched test structure

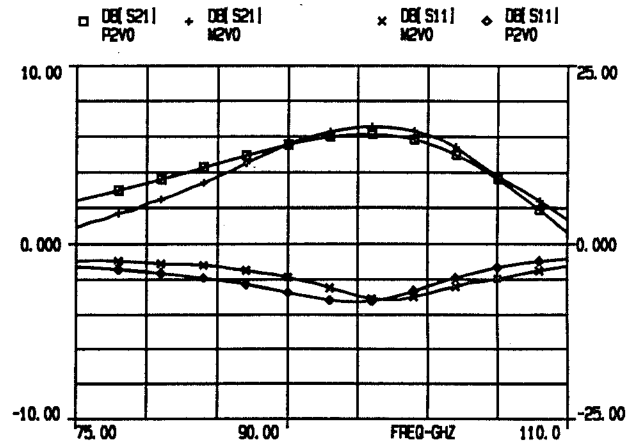

Fig. 2a Validation of the device model with the single-device test structure

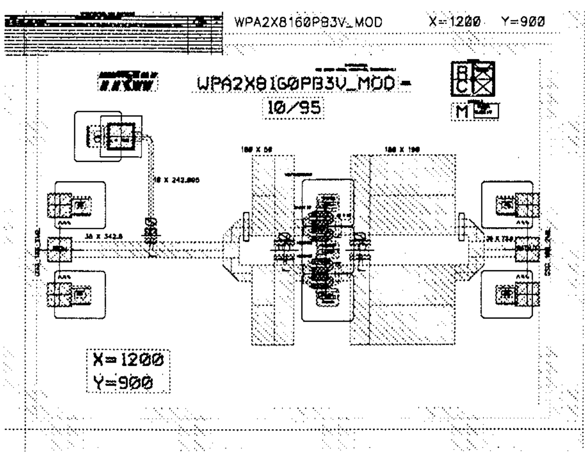

Fig. 1b Layout of the two-device pre-matched test structure

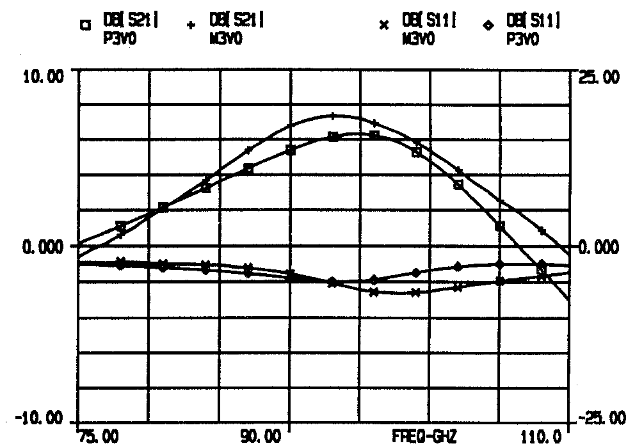

Fig. 2b Validation of the device model with the two-device test structure

design. The first stage employs 4 cells of 8-finger, 160-μm HEMTs and second stage has twice the device periphery with 8 HEMT devices. With a single-ended design, the chip measures only 2.3-mm by 1.8-mm. The chip photograph is shown in Fig. 3. The RF performance is optimized with reactive matching elements. The microstrip edge-coupled lines between both stages provide proper impedance transformation which produces a wide-band design and ensures performance repeatability. After the matching elements are determined, full-wave EM analysis is used for the passive structures to eliminate the uncertainties caused by the quasi-static models.

With MIM capacitors for dc blocking, radial stubs for RF bypass and shunt R-C in the biasing networks for low frequency stability, the chip is made to be completely on-wafer probable. A small resistor and a shunt quarter-wave short stub are placed in the input and output matching networks to remove the undesired out-of-band gain. Isolation resistors between every pair of paralleled devices are used to prevent possible oscillations due to the high transconductance of a large device periphery.

MEASUREMENT RESULTS

The PA was first tested on-wafer for dc screening and linear gain. Owing in large part to the GaAs process maturity, very high RF yield was achieved.

On a single wafer where 11 sites of PA are available, 10 sites show 7 to 10 dB linear gain from 88 to 94 GHz. The bias voltages for drain and gate are 4V and 0V, respectively. Figure 4 shows the on-wafer tested linear gain performance of all 10 sites from a single wafer. The PA chip was then tested in a WR-10 waveguide test-fixture for output power measurement at the same bias condition. As shown in Fig. 5, the PA exhibits a 24.8-dBm (300 mW) maximum output power and a peak power added efficiency of 10.5% at 94 GHz. With a slight decrease in output power, PAE can be improved to 12.2% by lowering the drain voltage on the first stage to 3V with a maximum output power of 24.6 dBm.

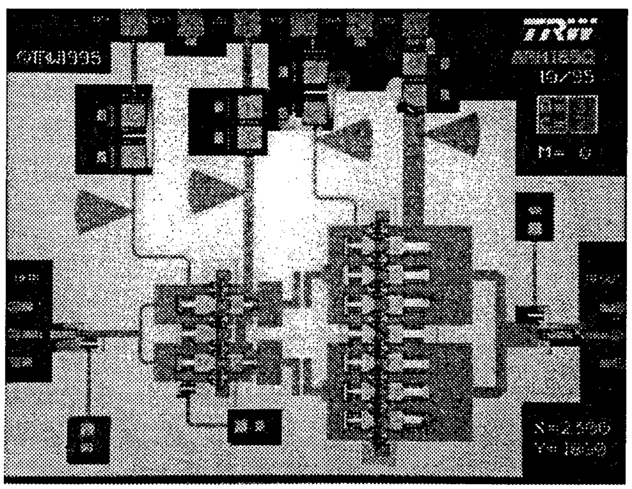

Fig. 3 The chip photo of the W-band monolithic power amplifier

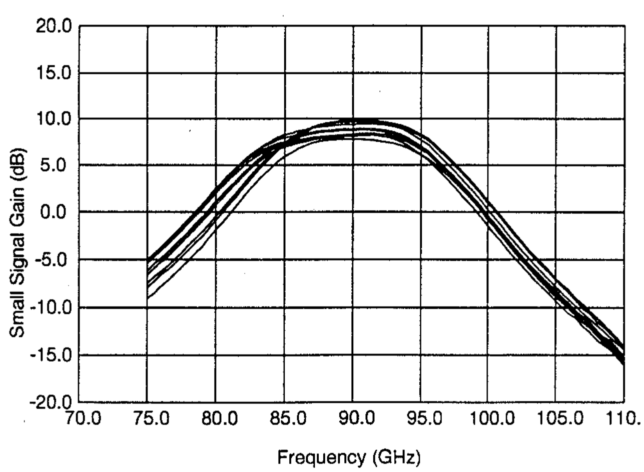

Fig. 4 The small signal gain of 10 different sites from 1 single wafer

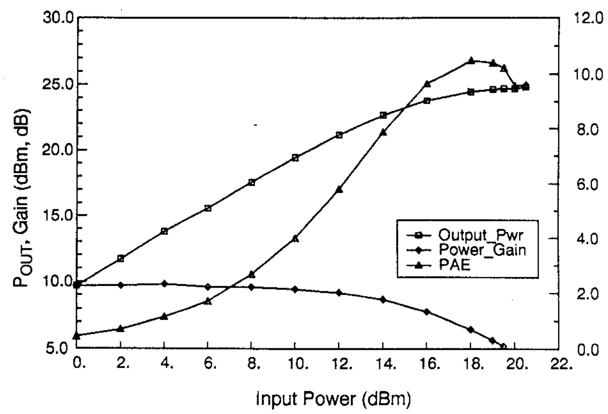

Fig. 5 P_{OUT} and power added efficiency vs. P_{IN} plots at 94 GHz

CONCLUSION

We have demonstrated a W-band MMIC two-stage power amplifier using 0.1-µm AlGaAs/InGaAs/GaAs power HEMT process on a 2-mil GaAs substrate in this paper. Excellent small-signal RF yield, 300mW output power and greater than 10% peak power-added efficiency have been achieved. This performance represents a breakthrough in monolithic millimeter wave PA design and demonstrates the maturity of power HEMT process capability.

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